DETAILED ACTION

Response to Arguments

The amendment filed on 03/14/2008 has been entered and considered by examiner.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1, 4-5, and 8-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada et al. (hereafter referenced as Asada), US Patent 5,883,609, in view of Wood et al. (hereafter referenced as Wood), US Patent 5,926,162.

Regarding claim 1, Asada discloses in figure 5 an image display device (10) comprising a plurality of gate buses (gate lines GP), a plurality of source buses (data lines DS), transistors (transistor shown in each pixel Px) each of which for supplying a pixel electrode (top electrode of pixel Px) with a voltage from said source bus, a common electrode (bottom electrode of pixel Px),

a changing voltage generating means (GP Pulses) for generating a first changing voltage having changing voltage levels for setting said transistor to an on-state and a second changing voltage having changing voltage levels for setting said transistor to an off-state (Since Asada's display is an active matrix, the gate pulses GP has both levels

to control ON, when gate pulse GP is high, and OFF, when gate pulse GP was low, of the transistors, so that image can be written, see timing charts in Fig. 8, 9, and 11),

said changing voltage generating means operating so as to establish at least three supply modes including a first supply mode, a second supply mode and a third supply mode (double, 4-fold, and 1.6-fold modes shown in Fig. 8, 9, and 11, respectively),

said first supply mode (double mode, Fig. 8) in which said first changing voltage is supplied to a first number of ones of said plurality of gate buses (GP1-GP2) and said second changing voltage is supplied to a second number of ones of said plurality of gate buses (GP3-GP1024) (a dual-line simultaneous scan during the double mode, for example, gate lines GP1 and GP2 are ON simultaneously while gate lines GP3-GP1024 are OFF in the first period of T during the image writing period, col. 16 lines 13-18),

said second supply mode (4-fold mode, Fig. 9) in which said first changing voltage is supplied to a third number of ones of said plurality of gate buses (GP1-GP4) and said second changing voltage is supplied to a fourth number of ones of said plurality of gate buses (GP5-GP1024) (a 4-line simultaneous scan during the 4-fold mode, for example, gate lines GP1-GP4 are ON simultaneously while gate lines G5-G1024 are OFF in the first period of T during the image writing period, col. 17 lines 4-9), and

said third supply mode (1.6-fold mode, Fig. 11) in which said first changing voltage is supplied to a fifth number of ones of said plurality of gate buses (GP2-GP3)

and said second changing voltage is supplied to a sixth number of ones of said plurality of gate buses (GP1 and GP4-GP1024) (a dual-line simultaneous scan in a single-line sequential scan during the 1.6-fold, for example, after gate line GP1 is ON, while gate lines GP2-GP1024 are off in the first period T during the image writing period, the next period T during the image writing period will turn ON gate lines GP2 and GP 3, while gate lines GP1 and GP4-GP1024 OFF, Fig. 11 in col. 18 lines 60-67);

But, Asada does not specifically teach a corrected voltage supplying means for supplying said common electrode with a common electrode voltage which has been corrected by an amount of correction and a corrected voltage generating means for detecting a voltage on said common electrode to determine said amount of correction on the basis of amounts of change in said detected voltages on said common electrode.

However, Wood teaches a corrected voltage supplying means (amplifier 512, Fig. 5 in col. 9 lines 22-32) for supplying said common electrode with a common electrode voltage which has been corrected by an amount of correction and a corrected voltage generating means for detecting a voltage on said common electrode to determine said amount of correction on the basis of amounts of change in said detected voltages on said common electrode (a parasitic capacitance compensation signal generator 402 generates a signal corresponding to the effect of the parasitic capacitances of the TFTs 208 on the gate drive signals Gn and adjusts the voltage applied to the common electrode 114, Fig. 5 in col. 7 lines 33-45). Thus combining Asada and Wood would meet the claimed limitation “a corrected voltage supplied means…” as recited in the claim.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have used the corrected voltage supplying means as taught by Wood to correct the common electrode during at least one of the three modes established by Asada for the purpose of reducing the inadvertent accumulation of a charge differential across the liquid crystal layer (col. 2 lines 56-62).

Regarding claim 4, Asada discloses wherein said corrected voltage supplying means comprises a predetermined voltage generating means (horizontal drive circuit 103) for generating a predetermined voltage to supply said source bus (source line DS) with said predetermined voltage,

and wherein said plurality of source buses are supplied with said predetermined voltage in each of said at least three supply modes (Asada teaches all three modes to be perform during the image writing period as shown in Fig. 8, 9, and 11, for example, in double mode the image data will be supplied to the respective pair of neighboring source buses with those gate lines activated and no image data will be supplied to the respective source buses with those scanning lines not activated within the image writing period, col. 16 lines 16-18).

Regarding claim 5, Asada discloses wherein said predetermined voltage generating means (horizontal drive circuit 103) generates a constant voltage as said predetermined voltage (gate buses that are not activated will have no image data supplied to the source lines respective to the gate lines as shown in Fig. 8, 9, and 11, therefore there would be a constant voltage of zero volt supplied to the source lines with gate lines that are OFF).

Regarding claim 8, Asada does not specifically discloses wherein said changing voltage generating means operates so as to establish said at least three supply modes when a power supply of said image display device is turned from off to on.

However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the changing voltage generating means operates so as to establish said at least three supply modes when a power supply of said image display device is turned from off to on for the purpose of adapting to a projector, TV, or computer as they can have different signal sources such as bandwidth, pixel number, and scan modes (Asada: col. 1 lines 18-54).

Regarding claim 9, Asada in view of Wood does not specifically discloses wherein said changing voltage generating means operates so as to periodically establish said at least three supply modes under the condition that an power supply of said image display device is in an on.

However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have changing voltage generating means operates so as to periodically establish said at least three supply modes under the condition that an power supply of said image display device is in an on-state for the purpose of adapting to a projector, TV, or computer as they can have different signal sources such as bandwidth, pixel number, and scan modes (Asada: col. 1 lines 18-54).

3. **Claims 2-3, 7, and 11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada, in view of Wood, and in further view of Kurz, US Patent 4,810,973.

Regarding claim 11, this claim differs from claim 1 in that the limitations “a first detection…”, “a storing means…”, and “a DA converting means…” are additionally recited.

Asada does not specifically teach the additional limitations “a first detection…”, “a storing means…”, and “a DA converting means...” as recited.

However, Kurz teaches in Fig. 1,

a first detection terminal (AD) for detecting a offset voltage (col. 2 lines 5-32);

a storing means (Control circuit ST) for storing a compensation voltage which is determined on the basis of amounts of change in the detected voltages of the offset voltage through said first detection terminal (col. 2 lines 33-45); and

a DA converting means (DA) supplied with said compensation voltage stored in said storing means (control circuit ST) as a digital signal, said DA converting means (DA) converting said supplied digital signal into an analog voltage and outputting said analog voltage to control SG (col. 2 lines 5-32). Thus combining Asada in view of Wood with Kurz would meet the additionally claimed limitations “a first detection…”, “a storing means…”, and “a DA converting means…”.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have used the offset voltage correction circuitry as taught by Kurz to detect and correct the common electrode during at least the three modes of Asada in view of Wood for the purpose of having the offset voltage be recompensated every time the equipment is turned on, which in turn lets the user avoid maintenance of the equipment (col. 3 lines 25-41).

Regarding claim 2, Kurz teaches wherein a corrected voltage generating means comprises (circuitry of Fig. 1):

an AD converting means (AD) for detecting a offset voltage as an analog voltage to convert said detected analog voltages into first digital signals (col. 2 lines 5-32);

an operation means (Control circuit ST) for determining amounts of change in said detected analog voltages from said first digital signals and determining said amount of correction on the basis of said determined amounts of change to output an digital signal representing said offset voltage which has been corrected by said determined amount of correction (compensation voltage, col. 2 lines 33-45);

a DA converting means (DA) for converting said digital signal outputted from said operation means into an analog voltage (col. 2 lines 5-32), and

a switching means (variable switch S) for switching between a first connection mode in which said offset voltage is connected to said AD converting means, when the switch is open, and a second connection mode in which said offset voltage is connected to said DA converting means, when the switch is closed (col. 2 lines 5-32).

Thus combining Asada in viewof Wood with Kurz would meet the limitation of the circuitry “an AD…”, “an operation…", “a DA…”, and “a switching…” to operate with the common electrode at least during one of the three modes.

Regarding claim 3, Kurz discloses wherein said corrected voltage generating means (circuitry of Fig. 1) comprises a storing means (Control circuit ST) for storing said corrected common electrode voltage (compensation voltage) represented by said digital

signal (offset voltage is converted to digital via AD converter) outputted from said operation means,

and wherein said DA converting means (DA) converts said corrected common electrode voltage (compensation voltage) stored in said storing means into an analog voltage, instead of converting said digital signal outputted from said operation means into an analog voltage (col. 2 lines 5-45).

Regarding claim 7, Kurz discloses wherein said AD converting means (AD) detects a on-voltage and a off-voltage (offset voltage) as an analog voltage and converts said detected analog voltage into a second digital signal (the second digital signal is the signal outputted from the AD converter, col. 2 lines 5-32),

and wherein said operation means (control circuit ST) determines said amounts of change from said first digital signal (the first digital signal is the signal outputted from the AD converter) and values of said on-voltage and said off-voltage from said second digital signal (the second digital signal is the next signal outputted from the AD converter when the variable switch S opens again), and determines said amount of correction (compensation voltage) on the basis of said determined amounts of change and said determined values of said on-voltage and said off-voltage (col. 2 lines 5-45).

Regarding claim 12, Kurz discloses wherein said corrected voltage generating means (circuitry of Fig. 1, col. 2 lines 5-32) comprises an switching means (variable switch S) for switching between a first connection mode (variable switch S opened) in which said common electrode (line that carries signal F) is connected to said first

detection terminal (AD) and a second connection mode (variable switch S closed) in which said common electrode (line that carries signal F) is connected to said DA converting means (DA).

Regarding claim 13, Asada discloses wherein said corrected voltage supplying means comprises a predetermined voltage generating means (horizontal drive circuit 103) for generating a predetermined voltage to supply said source bus (source line DS) with said predetermined voltage,

and wherein said plurality of source buses are supplied with said predetermined voltage in each of said at least three supply modes (Asada teaches all three modes to be perform during the image writing period as shown in Fig. 8, 9, and 11, for example, in double mode the image data will be supplied to the respective pair of neighboring source buses with those gate lines activated and no image data will be supplied to the respective source buses with those scanning lines not activated within the image writing period, col. 16 lines 16-18).

Regarding claim 14, Asada discloses wherein said predetermined voltage generating means (horizontal drive circuit 103) generates a constant voltage as said predetermined voltage (gate buses that are not activated will have no image data supplied to the source lines respective to the gate lines as shown in Fig. 8, 9, and 11, therefore there would be a constant voltage of zero volts supplied to then source lines with gate lines that are OFF).

4. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Asada, in view of Wood, and in further view of Yamaguchi et al. (hereafter referenced as Yamaguchi), US Patent 5,307,084.

Regarding claim 6, Asada in view of Wood discloses an image display device as claimed in claim 1,

Asada also discloses wherein said changing voltage generating means comprises:

a plurality of output circuits (NAND gate circuits 15-1 to 15-1024, Fig. 5 with timing charts in Fig. 8, 9, and 11), each of which provided for a respective one of said plurality of gate buses (gate lines GP1-GP1024), for selectively outputting an on-voltage (high level signal GP) of a constant value for setting said transistor to an on-state and an off-voltage (low level signal GP) of a constant value for setting said transistor to an off-state;

But, Asada in view of Wood does not specifically teach a signal generating circuit for generating a changing voltage signal which represents a predetermined changing voltage; and

a plurality of adders, each of which provided for a respective one of said output circuits, for adding said predetermined changing voltage to said on-voltage when said on-voltage is outputted from the corresponding output circuit to output said first changing voltage, and for adding said predetermined changing voltage to said off-voltage when said off-voltage is outputted from the corresponding output circuit to output said second changing voltage.

However, Yamaguchi teaches a signal generating circuits (distortion detection circuit 12) for generating a changing voltage signal (signal coming from feedback line 102) which represents a predetermined changing voltage (compensation voltage) (Fig. 14 in col. 12 lines 2-8); and

a plurality of adders (103 and 104), each of which provided for a respective one of said output circuits (seen in Fig. 4 with unnamed triangular element to the left of the adder circuit 103 and 104 inside power source circuit 4), for adding said predetermined changing voltage to said on-voltage when said on-voltage is outputted from the corresponding output circuit to output said first changing voltage, and for adding said predetermined changing voltage to said off-voltage when said off-voltage is outputted from the corresponding output circuit to output said second changing voltage (Compensation voltage generation circuit 9 sends compensation voltage via feedback line 102 into adders 103 and 104 and changing voltages V2 and V5, Fig. 14 in col. 12 lines 4-8). Thus combining Asada in view of Wood with Yamaguchi would meet the claimed limitations “a signal generating circuit…” and “a plurality of adders…”.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have used a signal generating circuit with a plurality of adder as taught by Yamaguchi to change gate voltages of Asada for the purpose of canceling the cross-talk which develops on cells on unselected scan electrode (col. 1 lines 64-68 to col. 2 lines 1-2).

5. **Claims 15 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada, in view of Wood, in further view of Kurz, and in further view of Yamaguchi.

Regarding claim 15, rejection is the same basis as rejected on above claim 6.

Regarding claim 16, Wood discloses wherein said corrected voltage supplying means (amplifier 512, Fig. 5 in col. 9 lines 22-32) comprises a second detection terminal (e.g. gate drive signal Gn, where n=2) for detecting said on-voltage and a third detection terminal (e.g. gate drive signal Gn, where n=3) for detecting said off-voltage, and

wherein Kurz discloses the storing means (Control circuit ST, col. 2 lines 33-45) stores said corrected common electrode voltage (compensation voltage), and

wherein Wood discloses the corrected common electrode voltage which is determined on the basis of said amounts of change in said detected voltages (parasitic capacitance compensation signal generator 402, Fig. 5 in col. 7 lines 33-60) on said common electrode through said first detection terminal (e.g. gate drive signal Gn, where n=1), a value of said detected on-voltage through said second detection terminal (e.g. gate drive signal Gn, where n=2), and a value of said detected off-voltage through said third detection terminal (e.g. gate drive signal Gn, where n=3) (col. 7 lines 33-60)

Thus the combination of Wood supplying the corrected voltage base on multiple detected voltages via detection terminals and using the storage of Kurz to store the corrected voltages would meet the claimed limitations.

Allowable Subject Matter

6. Claims 10 and 17 are allowed.

Response to Arguments

7. Applicant's arguments filed 03/14/2008 have been fully considered but they are not persuasive.

Regarding claims 1 and 11, on page 15 of first paragraph, Applicant argues "the Section 103 rejections over Asada, Wood, Kurz, and Yamaguchi are believed to be improper… to modify the corrected voltage generating means…". However, Examiner disagrees with Applicant, each reference provides motivation as mentioned in the above rejection.

On page 16 of mid section, Applicant argues "Asada and Wood do not suggest the corrected voltage generating means for supplying said common electrode with a common electrode voltage which has been corrected by an amount of correction and corrected voltage generating means for detecting a voltage on said common electrode to determine said amount of correction on the basis of amounts of change in said detected voltages on said common electrode, as set forth in present claim 1." However, Examiner disagrees with Applicant, as described in the Wood reference in col. 7 lines 33-45,the compensation signal generator 402 generates a compensation signal on the gate drive with signal Gn. The compensation signal generator detects the voltage of the gates and sources of the TFTs 208 to determine the amount of compensation signal Gn to apply. Wood points out that the common electrode voltage is inversely proportional to the magnitude of the gate drive signal Gn, col. 7 lines 38-41, therefore by detecting the voltage of the gate lines is also detecting the common electrode, although the compensation signal generator 402 is not directly detecting the common electrode itself but indirectly as Wood discloses that the relationship is inversely proportional thereby being able to adjust the voltage applied to the common electrode 114, col. 7 lines 44-45.

On Page 21 of first paragraph, Applicant argues "Kurz does not disclose that the AD is capable of detecting the voltage on the common electrode...", however the combination in view of Kurz is used because Kurz taught the using the AD to detect offset voltage, therefore when the AD detects the common electrode as disclosed by Wood the offset voltage can be compensated, col. 3 lines 29-32.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BAO-QUAN T. HO whose telephone number is (571)270-3264. The examiner can normally be reached on M-F, 8:30 am to 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh D. Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTH

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